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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE PATENT TRIAL AND APPEAL BOARD

Ex parte ROBERT STEINHOFF, JONATHAN S. BRODSKY, and THOMAS A. VROTSOS

Appeal 2009-010379
Application 09/498,677
Technology Center 3600

Before JOHN C. KERINS, MICHAEL C. ASTORINO, and JAMES P. CALVE, *Administrative Patent Judges*.

KERINS, *Administrative Patent Judge*.

DECISION ON APPEAL

STATEMENT OF THE CASE

Robert Steinhoff *et al.* (Appellants) seek our review under 35 U.S.C. § 134 of the Examiner's final rejection of claims 1-13. Claims 14-45 have been canceled. We have jurisdiction under 35 U.S.C. § 6(b). We AFFIRM-IN-PART.

THE INVENTION

Appellants' invention is directed to a structure, disclosed in the Specification as being suitable for use as a bi-directional protection circuit. Spec. 1, ll. 11-12. Independent claim 1 is illustrative:

> 1. A structure comprising:
>
> an external terminal;
>
> a reference terminal;
>
> a first transistor formed on a substrate, the first transistor having a current path electrically connected between the external terminal and the reference terminal;
>
> a second transistor having a current path electrically connected between the external terminal and the substrate; and
>
> a third transistor having a current path electrically connected between the substrate and the reference terminal, wherein the current paths of the second and third transistors are in parallel with the current path of the first transistor.

THE REJECTIONS

The Examiner has rejected:

(i) claims 1, 2, 6, 7, 11, and 12 under 35 U.S.C. § 102(e) as being anticipated by Williamson (US 6,369,427 B1, iss. Apr. 9, 2002);

(ii) claims 3-5, 8-10, and 13 as being unpatentable over Williamson in view of Williams (US 6,060,752, iss. May 9, 2000); and

(iii) claim 13 as being unpatentable over Williamson in view of Maeda (US 5,976,921, iss. Nov. 2, 1999).

ANALYSIS

Anticipation--Claims 1, 2, 6, 7, 11, and 12--Williamson

The Appellants separately argue claims 1, 2, and 6. *See* 37 C.F.R. § 41.37(c)(1)(vii) (2011).

With respect to claim 1, the Examiner found that Williamson discloses all the elements in claim 1 including "a second transistor having a current path electrically connected between the external terminal and the substrate" and "a third transistor having a current path electrically connected between the substrate and the reference terminal." Ans. 5-6; App. Br., Clms. App. The Examiner relies upon Williamson's Figures 5 and 6, taking the position that p-type and n-type transistors *44* are each electrically connected to the substrate *60* through resistor *42*, node *66*, and the source/drain regions *62* and *63* of first transistor *56*.[1] Ans. 5, 6, and 12-14. The Appellants counter that they believe the "Examiner has interpreted substrate

[1] We note that diffusion regions *62* and *63* are doped regions of silicon that are part of silicon substrate *60*. Williamson, col. 6, ll. 32-38.

connections recited in claim 1 as capacitive coupling between source or drain regions of the p-type and n-type transistors in 44." App. Br. 4.

The Appellants' argument that the Examiner relied upon a capacitive coupling condition is misplaced. Despite the Examiner's mention of capacitive coupling in the rejection of claim 6, the Examiner did not rely upon capacitive coupling as the basis for finding that the current paths recited in claim 1 were present in Williamson. *See* Ans. 5-6, 14. The Examiner discussed "capacitive coupling" only with respect to the rejection of claims 6 and 12. Ans. 6-7. Since all of the Appellants' arguments with respect to claim 1 are premised on the Examiner's reliance upon a "capacitive coupling" condition, the rejection of claim 1, and of dependent claim 11 grouped therewith, as anticipated by Williamson is sustained.[2]

With respect to claim 2, the Examiner found that Williamson discloses all the elements in claim 2, including a first and second resistor. Ans. 6. The Examiner took the position that the first and second resistors are located within Williamson's transistors *44*, describing these resistors as "contact resistance caused by the contact made between the gate and the source/drain." Ans. 6, 15-16. The Appellants counter that contact resistance is not a resistor, and as a result, the Examiner has failed to recite a first and second resistor. App. Br. 5-6.

By relying upon contact resistance, rather than a resistor element as required by the Appellants' claim 2, the Examiner adopted an unreasonably broad interpretation of a resistor. When interpreting the breadth of claim

[2] Appellants also argue that the "Examiner omits key parts of claim 1" but Appellants do not identify any deficiencies in the Examiner's findings in this regard. Appellants only present arguments regarding the connections of the first and second transistors and the substrate. App. Br. 4-5.

language, we apply the broadest reasonable meaning of the terms in their ordinary usage as they would be understood by one of ordinary skill in the art, taking into account whatever enlightenment by way of definitions or otherwise that may be afforded by the written description. *See In re Morris*, 127 F.3d 1048, 1054 (Fed. Cir. 1997). In this case, although the Appellants' disclosure provides no specific definition of a "resistor," the Specification applies the term "resistor" consistent with traditionally known resistor elements, and similarly, the Drawings illustrate resistor elements rather than resistance representations. Spec., p. 6, ll. 15-20; Fig. 1A, items 114 and 116. Based upon the Appellants' disclosure, we find that one of ordinary skill in the art would not recognize contact resistance within a transistor to be a "resistor" as disclosed and claimed by the Appellants.

Furthermore, with respect to claim 2, the Appellants' disclosure undermines the Examiner's position of the resistors being part of the transistors, by clearly distinguishing between a "transistor" and a "resistor." Spec., p. 6, ll. 15-20; Figs. 1A and 2A. Consistent with the principle that all limitations in a claim must be considered to be meaningful, it is improper to rely on the same structure in the Williamson reference as being responsive to two different elements (transistor and resistor). *See, Lantech, Inc. v. Keip Mach. Co.*, 32 F.3d 542, 546-47 (Fed. Cir. 1994) (in infringement context, a single conveyor held to not meet claim element requiring at least two conveyors); *In re Robertson*, 169 F.3d 743, 745 (Fed. Cir. 1999) (claim requiring three separate means not anticipated by structure containing two means where one of the two means was argued to meet two of the three claimed means). We find that the Examiner improperly construed Williamson's transistors *44* as both a transistor and a resistor.

Based upon the Examiner's impermissibly broad interpretation of the term "resistor" shown above and the Examiner's interpretation of the Williamson's transistor *44* as both a transistor and a resistor, the rejection of claim 2 as anticipated by Williamson is not sustained.

With respect to claims 6 and 12, the Examiner found that Williamson discloses all the elements of claim 1 including a control terminal electrically connected to the substrate. Ans. 6-7. The Examiner cited to gate *67* of Williamson's transistor *56* as being responsive to the claimed control terminal, asserting that gate *67* is electrically connected to substrate *60* via capacitive coupling. *Id.* The Appellants counter that reliance on capacitive coupling to meet the claim limitation calling for the control terminal to be electrically connected to the substrate improperly construes the claim language. App. Br. 6.

We agree with Appellants the term "electrically connected" would not be construed in its broadest reasonable interpretation as including a capacitive coupling between the control terminal and the substrate of Williamson, as maintained by the Examiner. The Specification does not expressly provide a definition of the term "electrically connected." Nonetheless, the Specification does shed light on the meaning that would be conveyed to persons of ordinary skill in the art by employing the terms "electrical connection" and "capacitively coupled."[3] Persons having

[3] The Specification sets forth that "[t]he control gate 126 of MOS transistor 106 is connected to P+ region 132 by first metal 108 and respective contacts. This P+ region 132 *electrically connects* the control gate 126 to the P-well region 171." Spec., p. 5, ll. 26-28 (emphasis added). The Specification impliedly contrasts that term with "capacitive coupling" in discussing that "[d]uring ESD operation, application of a positive ESD pulse to bond pad

ordinary skill in the electrical art would understand, from reading these and other similar passages in the Specification, that Appellants intended that the terms "electrically connected" and "capacitively coupled" be interpreted as describing two different conditions or arrangements. As such, the Examiner's rejection that relies on a capacitive coupling as providing the claimed electrical connection is in error. The rejection of claims 6 and 12, and of claim 7 depending from claim 6 and grouped therewith, as anticipated by Williamson, is not sustained.

Obviousness--Claims 3-5, 8-10, and 13--Williamson/Williams

The Appellants presented no arguments responding to the Examiner's rejection of claims 3 and 13 over Williamson and Williams. We therefore summarily affirm the rejection of claims 3 and 13.

With respect to claim 4, the Examiner acknowledges that Williamson "*does not necessarily teach*" the limitations set forth in these claims. Ans. 8. The Examiner cites to the Williams patent as teaching a first heavily doped region *926* or *928* ("NBL region") having a second conductivity type ("n-type") and a second lightly doped region 904 also of the second conductivity type, which region is formed at the face of the substrate and extends to the first heavily doped region. *Id.*; Williams, Fig. 9A. The Examiner concluded that it would have been obvious to provide the Williamson apparatus with a first heavily doped region having a second conductivity type underlying the substrate and transistor and a second lightly doped region extending from the

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100 with respect to reference terminal 102 *capacitively couples* a positive voltage via parasitic gate-drain capacitance (not shown) of transistor 106 to lead 108." Spec., p. 6, ll. 22-24 (emphasis added).

face of the substrate to the first heavily doped region to provide diode protection through doping of the substrate. *Id.* The Appellants contend that, in Williams, there is no first transistor formed on substrate *900*, and further that the first heavily doped region (NBL Layer *926* or *928*) does not underlay the substrate. App. Br. 7.

We are not persuaded of Examiner error by either argument. The Examiner relied on Williamson as teaching the first transistor, Williams was relied on as teaching the recited doped regions. Ans. 17-18. The combined teachings result in the doped regions underlying a first transistor. As to the Appellants' second argument, Williams' first heavily doped region *926* or *928* is positioned, in a manner similar to the heavily-doped diffusion under field 170 in the Appellants' disclosed structure, underlying a portion of the P-epitaxial portion *902* of the substrate *900* in Williamson. Williams, Fig. 9A; col. 6, l. 51 to col. 7, l. 7. The rejection of claim 4, and of dependent claim 5 grouped therewith, as being unpatentable over Williamson in view of Williams is sustained.

Claims 8-10 depend from claim 6, for which the anticipation rejection in view of Williamson was not sustained. Even though the Appellants' arguments for claim 8 are the same as those found unpersuasive for claim 4, the additional reliance on Williams does not remedy the deficiency in Williamson noted in the analysis of the rejection of claim 6 above. As such, the rejection of claims 8-10, as being unpatentable over Williamson in view of Williams is not sustained.

Obviousness--Claim 13--Williamson/Maeda

The Examiner takes the position that Williamson "does not necessarily" disclose that the first transistor is a bipolar transistor, as called for in claim 13. Ans. 10. The Examiner cites to the Maeda patent as teaching a semiconductor-based ESD protection device employing MOS transistors and a bipolar transistor. Maeda, col. 13, ll. 48-65. The Examiner concluded that it would have been obvious to modify Williamson in view of Maeda such that the first transistor of Williamson is a bipolar transistor, to enable escape of excessive current and voltage. *Id.*

The Appellants maintain that Maeda discloses "a vertical NPN transistor of a BiCMOS process" and that "[t]he BiCMOS process of Maeda is incompatible with the CMOS process of Williamson." App. Br. 7. The Appellants thus argue that one of ordinary skill in the art would not think to combine elements from two incompatible processes in arriving at the subject matter of claim 13. *Id.*

The Examiner counters that claim 13 involves a structure or device, and not a process. Ans. 19. The Examiner further explains that Maeda evidences that MOS transistors and bipolar transistors can both be combined in an ESD protection device substrate. *Id.* We believe that the Examiner has the better position here. The Appellants' arguments appear to be founded on the premise that the Examiner is proposing to bodily incorporate not only the bipolar transistor of Maeda into the Williamson device, but also the process by which it is produced.

The Appellants additionally argue that there is "no teaching or suggestion in either reference to indicate how or why the second and third series-connected transistors of claim 13 might have current paths connected

to the base of the first transistor and in parallel with a current path of the first transistor." App. Br. 8. The Examiner replies that the only modification proposed in this rejection is the selection of another type of transistor for the first transistor. We are not persuaded by the Appellants' argument that the Examiner erred in making this rejection.

The rejection of claim 13 as being unpatentable over Williamson in view of Maeda is sustained.

CONCLUSIONS

The Examiner did not err in finding that the subject matter of claims 1 and 11 is anticipated by Williamson. The Examiner erred in finding that the subject matter of claims 2, 6, 7, and 12 is anticipated by Williamson.

The Examiner did not err in concluding that the subject matter of claims 4 and 5 would have been obvious over Williamson and Williams.

The Examiner did not err in concluding that the subject matter of claim 13 would have been obvious over Williamson and Maeda.

DECISION

The rejection of claims 1 and 11 as being anticipated by Williamson is affirmed. The rejection of claims 2, 6, 7, and 12 as being anticipated by Williamson is reversed.

The rejection of claims 3-5, 8-10, and 13 as being unpatentable over Williamson and Williams is affirmed.

The rejection of claim 13 as being unpatentable over Williamson and Maeda is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a)(1)(iv).

AFFIRMED-IN-PART

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